FINAL TECHNICAL REPORT

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DEVELOPMENT OF INFRARED DETECTION TECHNIQUES

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INTRODUCTION

The principle objective of this research project has been to develop a family of low-temperature readouts for use with germanium infrared detectors in space applications. These readouts are essential if space projects such as SIRTF are to achieve their full potential at infrared wavelengths from 40 to 200 microns. Very briefly, the technical requirements are the following: (a) stable operation at temperatures below 4 K (b) low-noise in the simple integrator mode of operation to satisfy the need for continuos sampling of the signals from Ge photoconductors and (c) low power dissipation to enable large numbers of detectors to be operated simultaneously.

At the conclusion of this project we have tested numerous devices that meet all 3 technical requirements as stated above. There appear to be no remaining questions or issues that would prevent the SIRTF mission from utilizing this new technology to construct large flight qualifiable arrays of Ge detectors. In addition to meeting the specific requirements of the MIPS instrument in SIRTF we believe that this new readout technology may be applicable to many other projects that need to operate IR detectors at very low temperatures.

PROJECT SUMMARY

A brief review is given here of the main activities that were accomplished.

At the outset of this project it was realized that Bill Kleinhans had proven the basic concept of a cryogenic MOSFET transistor capable of stable operation at temperatures well below the freeze-out temperatures of doped silicon. Discussions with Bill Kleinhans concluded that his designs would form the most suitable basis for finding a workable solution to the well known problems of dc-instability and excess noise found in almost all circuitry using standard CMOS devices at temperatures below 30 K. Working with him and building on our knowledge of the simple integrating amplifier and multiplexer used by use previously to build a 1x16 JFET readout we designed a 1x32 linear readout chip that could be produced by the TRW foundry and that could be used to construct 32x32 arrays of Ge photoconductors operating below 2 K.

In addition to the actual 1x32 readout chip we included on the wafers a number of test devices and unit cells specifically designed to study specific issues including: (a) contact noise (b) geometry (c) noise vs. area and (d) reset switch functionality. We also divided the run into 3 splits to study the effects of different starting material.

The first TRW run was only partly successful due to an accident in the processing. However, we did find that some of the test devices escaped degradation in the accident and our tests of these samples demonstrated all of the characteristics that were needed. This key information showed which material to use and defined the optimum geometry. These very early devices still represent the lowest noise and most stable operation of any unit cells tested to date.

Unfortunately, the second run at TRW was less successful than the first and the foundry was closed before the third and final run could be carried out.

Efforts to transfer the TRW process to the foundry at Orbit also proved only partly successful.

We then shifted our efforts to the Hughes foundry at Carlsbad, CA (Hughes Technology Center, HTC) where cryogenic devices for SBRC were then carried out. Based on the prior work with Bill Kleinhans we designed new circuits and devices at HTC. These runs ultimately proved successful. At first we found that the standard HTC cryogenic CMOS devices were unstable and were subject to variable noise at relatively high levels. The main conclusion that was reached is that if the optimum geometry and doping levels found at TRW are applied to the Hughes process then their device design and processing produces comparable test results.

Extensive test and characterization of the Hughes MOSFET test devices prove that when operated at temperatures from 4.5 K to 2 K their devices are both stable and low-noise. Power dissipation is about 1 microwatt for optimum performance.

We compared our test results to a simple model that predicts open gate noise from shorted gate noise and found satisfactory agreement.

CONCLUSIONS

Simple dc integrating readout devices can be designed using well established CMOS design rules and starting epitaxial material where the substrate is degenerate and the epi-layer is fully depleted at 4 K. Readnoise of 30 e- with ~1 pf input capacitance can be routinely achieved.